## REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1-16 are in this case. Claims 1-16 have been rejected under § 102(b). Independent claims 1, 15 and 16 have been amended.

The claims before the Examiner are directed toward an electronic module that includes electronic circuitry and first and second electrical connection mechanisms, both operationally connected to the electronic circuitry, for mounting the module on a printed circuit board by different respective methods. The module needs to be mounted using only one of the electrical connection mechanisms in order to be fully operational.

### § 102(b) Rejections – Chillara et al. '955

The Examiner has rejected claims 1-4, 6, 13, 15 and 16 under § 102(b) as being anticipated by Chillara et al., US Patent No. 5,569,955 (henceforth, "Chillara et al. '955"). The Examiner's rejection is respectfully traversed.

Chillara et al. '955 teach integrated circuit assemblies such as integrated circuit assembly **30** that includes an IC chip **44** with input/output pads **46**. Some input/output pads **46** are connected to respective leadframe leads **48** by bonding wires **56**. Other input/output pads **46** are connected to respective solder balls **42** by bonding wires **58** and conductive traces **40**.

Leadframe leads **48** and solder balls **42** are different electrical connection mechanisms for mounting integrated circuit assembly **30**. Because each input/output pad **46** is connected either to a leadframe lead **48** or to a solder ball **42** but not to both a leadframe lead **48** and a solder ball **42**, integrated circuit assembly **30** must be

mounted using both leadframe leads **48** and solder balls **42** in order to be fully operational. If integrated circuit assembly **30** is mounted using only leadframe leads **48** then whatever circuitry in IC chip **44** that needs the input/output pads **46** that are connected to solder balls **42** is not operational. If integrated circuit assembly **30** is mounted using only solder balls **42** then whatever circuitry in IC chip **44** that needs the input/output pads **46** that are connected to leadframe leads **48** is not operational.

By contrast, the electronic module of the present invention is fully operational when mounted using either the first electrical connection mechanism or the second electrical connection mechanism. For example, module **30** of Figures 7-9 of the above-identified patent application is fully operational whether mounted using only BGA **1** or plug **2** because the solder balls of BGA **1** are electrically connected to the pads of plug **2** by wires **7**.

While continuing to traverse the Examiner's rejections, Applicant has, in order to expedite the prosecution, chosen to amend independent claims 1, 15 and 16 in order to clarify and emphasize the crucial distinctions between the electronic module of the present invention and the integrated circuit assembly of Chillara et al. '955. Specifically, claims 1, 15 and 16 have been amended to clarify that the electronic module of the present invention needs to be mounted using only one of the two connection mechanisms to be fully operational. Support for this amendment is found in the specification in Figures 7-9 and the accompanying text as described above. Because the solder balls of BGA **1** are electrically connected to the pads of plug **2** by wires **7**, it is inherent in module **30** that module **30** is fully operational whether mounted using only BGA **1** or only plug **2**.

Furthermore, the present invention, as recited in independent claims 1, 15 and 16 as now amended, is not even obvious from Chillara et al. '955. Chillara et al. '955

are careful to keep their two electrical connection mechanisms insulated from each other, for example by using dielectric layer **50** to separate leadframe leads **48** from conductive traces **40**. There is neither a hint nor a suggestion in Chillara et al. '955 of any utility to arranging any one of input/output pads **46** to be mountable using either a leadframe lead **48** or a solder ball **42**, let alone to having all the input/output pads **46** mountable using either leadframe leads **48** or solder balls **42**.

With independent claim 1 allowable in its present form it follows that claims 2-4, 6 and 13 that depend therefrom also are allowable.

**§ 102(b) Rejections – Farnsworth et al. '629**

The Examiner has rejected claims 1-3 and 5-13 under § 102(b) as being anticipated by Farnsworth et al., US Patent No. 6,020,629 (henceforth, "Farnsworth et al. '629"). The Examiner's rejection is respectfully traversed.

Farnsworth et al. '629 teach a semiconductor package **14** that includes several stacked substrates **12**. Each substrate **12** includes a semiconductor die **20**, each of whose die bond pads **34** is electrically connected to a contact pad **40** on the top side of substrate **12** and to an external contact **42** on the bottom side of substrate **12**. Each substrate **12** except the topmost substrate **12** is electrically connected via its contact pads **40** to external contacts **42** of the substrate **12** immediately above. As described in column 9 lines 2-5, semiconductor package **14** as a whole is mounted on a printed circuit board using only external contacts **42** of the bottommost substrate **12**. In other words, semiconductor package **14** has only one connection mechanism for mounting semiconductor package **14** on a printed circuit board. Therefore, Farnsworth et al. '629 has nothing whatsoever to do with the present invention as recited in independent claim 1.

With independent claim 1 allowable over Farnsworth et al. '629 in its present form it follows that claims 2, 3 and 5-13 that depend therefrom also are allowable.

**§ 102(b) Rejections – Hsu '133**

The Examiner has rejected claims 1, 13 and 14 under § 102(b) as being anticipated by Hsu, US Patent No. 5,481,133 (henceforth, "Hsu '133"). The Examiner's rejection is respectfully traversed.

Hsu '133 teaches a multichip array package in which substrates **26** that have "interconnected integrated circuit elements...thereon" (column 2 lines 49-50) are stacked and electrically connected to each other, and to an underlying substrate **20** that has "integrated circuit elements...fabricated in at least the central portion of the substrate" (column 2 lines 17-18), by conductive material **46** in openings **42**. Terminal pads **24** of substrate **20** are connected to lead frame terminals **48** by Au wires **50**. (Applicant notes in passing that the Examiner misinterpreted reference numeral **48** of Hsu '133 as referring to "electronic circuitry", presumably because substrate **20** is mislabeled in Figure 5 with reference numeral **48**.)

Like semiconductor package **14** of Farnsworth et al. '629, the multichip array package of Hsu '133 has only one connection mechanism, lead frame terminals **48**, for mounting the multichip array package on a printed circuit board. Therefore, Hsu '133 has nothing whatsoever to do with the present invention.

With independent claim 1 allowable over Hsu '133, it follows that claims 13 and 14 that depend therefrom also are allowable.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1, 15 and 16, and hence dependent claims 2-14 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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